In re Patent Application of:
ALIA ET AL.
Serial No. **10/010,738**
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In the Claims:

Claims 1 to 11 (Cancelled).

12. (Currently Amended) A system-on-chip (SOC) comprising:

a plurality of circuit blocks, each responsive to a respective local clock signal;

a system clock connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals;

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; ~~and~~

each circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal to said power control ~~manager.~~ manager;

said power control manager being connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom, said power control manager comprising

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals, and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown

acknowledgment signals; and

a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

13. (Previously Presented) An SOC according to Claim 12, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

Claim 14 (Cancelled).

15. (Currently Amended) An SOC according to ~~Claim 14~~ Claim 12, wherein each circuit block further comprises a block logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

16. (Currently Amended) An SOC according to ~~Claim 14~~ Claim 12, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown

signal, the shutdown acknowledgment signal and the system clock signal.

Claims 17-18 (Cancelled).

19. (Previously Presented) An SOC according to Claim 12, further comprising another system clock connected to selected circuit blocks for providing a system clock signal thereto.

20. (Currently Amended) A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto; ~~and~~

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising

a block logic circuit having an input for receiving the shutdown signal, and an output for providing a shutdown acknowledgment signal to said power control manager after receiving the shutdown signal, and

a shutdown circuit connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal after said block logic circuit provides the shutdown acknowledgment signal to said power control ~~manager.~~ manager;

said power control manager being connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom, said power control manager comprising

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals, and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals; and

central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

21. (Previously Presented) An SOC according to Claim 20, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

Claim 22 (Cancelled).

23. (Currently Amended) An SOC according to ~~Claim 22~~ Claim 20, wherein each block logic circuit is connected to said shutdown circuit through the respective power down

request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

24. (Currently Amended) An SOC according to ~~Claim 22~~ Claim 20, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

Claims 25-31 (Cancelled).

32. (Currently Amended) A method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks, and a power control manager, the method comprising:

providing a system clock signal to the circuit blocks for functioning as a respective local clock signal;

selectively providing a shutdown signal from the power control manager to the circuit blocks; ~~and~~

preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment ~~signal.~~ signal;

each circuit block comprising a shutdown circuit connected to the power control manager through a respective power down request line for receiving the shutdown signal

therefrom, and through a respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto;

the power control manager comprising a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals, and a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals; and

determining whether each circuit block is in an active state or an idle state by querying the first and second registers.

33. (Previously Presented) A method according to Claim 32, further comprising preventing the system clock signal from functioning as the respective local clock signal if the corresponding circuit block receiving the shutdown signal is in an idle state.

Claim 34 (Cancelled).

35. (Currently Amended) A method according to ~~Claim 34~~ Claim 32, wherein each circuit block further comprises a block logic circuit connected to the shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

36. (Currently Amended) A method according to ~~Claim 34~~ Claim 32, wherein each shutdown circuit comprises a logic

circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to a system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

Claims 37-38 (Cancelled).